UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/712,873	11/15/2000	Jason D. Kridner	TI-29077	9315

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EXAMINER
NALVEN, ANDREW L

ART UNIT	PAPER NUMBER
2134	

NOTIFICATION DATE	DELIVERY MODE
10/22/2007	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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	Application No.	Applicant(s)
Office Action Summary	09/712,873	KRIDNER, JASON D.
	Examiner	**Art Unit**	
	Andrew L. Nalven	2134	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) FROM
THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed
  after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
  Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any
  earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 August 2007*.

2a)☐ This action is **FINAL**.   2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is
closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 September 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☐ All   b)☐ Some * c)☐ None of:

        1.☐ Certified copies of the priority documents have been received.

        2.☐ Certified copies of the priority documents have been received in Application No. _____.

        3.☐ Copies of the certified copies of the priority documents have been received in this National Stage
application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
    Paper No(s)/Mail Date _____.

4) ☒ Interview Summary (PTO-413)
    Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1.   Claims 1-23 are pending.

Response to Arguments

2.   Applicant's arguments with respect to claims 1-20 have been considered but are moot in view of the new ground(s) of rejection.

3.   Applicant argues that DeLuca fails to teach determining an authorization state by comparing a mathematical function result executed by the digital signal processor to an expected result. Examiner respectfully disagrees. DeLuca teaches determining an authorization state by comparing a mathematical function result executed by the digital signal processor to an expected result (DeLuca, column 6 lines 41-49, does compare operation to determine if there is a match). DeLuca teaches a mathematical function by teaching a comparison operation. All computer functions are mathematical functions. Thus, the comparison of two values in order to determine a match by a computer is thus a mathematical function. As a result, Examiner maintains that DeLuca teaches determining an authorization state by comparing a mathematical function result executed by the digital signal processor to an expected result.

Claim Rejections - 35 USC § 103

4.   The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set
> forth in section 102 of this title, if the differences between the subject matter sought to be patented and
> the prior art are such that the subject matter as a whole would have been obvious at the time the
> invention was made to a person having ordinary skill in the art to which said subject matter pertains.
> Patentability shall not be negatived by the manner in which the invention was made.

5.   Claims 1-18 and 21-22 are rejected under 35 U.S.C. 103(a) as being

unpatentable over DeLuca et al US Patent No 5,612,682 in view of Seo et al US Patent

No 5,063,597, Tran US Patent No. 5,734,729, and Nagata US Patent No. 6,114,981.

6.   With regards to claims 1 and 12, DeLuca teaches a digital signal processor

(DeLuca, column 4 lines 59-67) operable to provide digital data output (DeLuca, column

7 lines 34-38), determines an authorization state by comparing a mathematical function

result executed by the digital signal processor to an expected result (DeLuca, column 6

lines 41-49, does compare operation to determine if there is a match), and generate a

disable signal (DeLuca, column 6 lines 49-52). DeLuca fails to teach a digital to analog

converter operable to receive the disable signal and the disable signal being generated

when a sleep condition is met. Seo teaches a digital to analog converter (Seo, column

3 lines 32-38) coupled to a digital signal processor and operable to receive the digital

data output (Seo, Figure 4 Items 41 and 40), convert the digital data to corresponding

analog data (Seo, column 3 lines 32-38), output the corresponding analog data (Seo,

column 3 lines 32-38, Figure 2C), mute the output of the corresponding analog data

(Seo, column 3 lines 32-38), receive the disable signal (Seo, column 3 lines 32-34), and

mute the output of the corresponding analog data in response to the disable signal

(Seo, Figures 2B and 2C, column 3 lines 14-38). Nagata teaches a digital to analog

converter including an input operable to receive the disable signal (Nagata, column 4 lines 28-49, D/A converter with mute control, Figure 3, column 1 lines 51-61). Tran teaches a disable signal generated when the electronic device satisfies one or more sleep conditions (Tran, column 2 lines 34-42). At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to utilize Seo's method of muting in response to a disable signal, Tran's method of disabling when a sleep condition is met, and Nagata's placement of the disable signal with DeLuca's communication device because it offers the advantage of providing an improved muting system that limits disturbing noises that are generated during the process of turning off power to the system or by external influences (Nagata, column 1 lines 35-50) and the reduction of transient noises associated with shutdowns or sleep modes (Tran, column 2 lines 34-42).

7.   With regards to claims 2, 10 and 15, DeLuca as modified teaches the authorization state either being positive or negative (DeLuca, column 6 lines 42-52) and further teaches the digital signal processor operative to generate the disable signal when the authorization state is negative (DeLuca, column 7 lines 2-7).

8.   With regards to claim 3, Deluca as modified teaches the serial input for receiving timing signals to enable reception of the disable signal (Seo, column 3 lines 55-58).

9.   With regards to claims 4 and 13, DeLuca as modified teaches the output muted by filtering the received digital data prior to conversion into analog data (Seo, column 3 lines 3-31).

10.   With regards to claim 5, DeLuca as modified teaches the output pin operable to
transmit the disable signal as a high voltage (Seo, column 3 lines 50-51).

11.   With regards to claim 6 (as best understood), DeLuca as modified teaches the
output pin operable to transmit a low voltage in the absence of a disable signal (Seo,
column 3 lines 50-54).

12.   With regards to claims 7 and 11, DeLuca as modified teaches the authorization
state is either positive or negative and the DSP is not operable to generate the disable
signal when the authorization state is negative (DeLuca, column 10 lines 15-24).

13.   With regards to claims 8 and 16-17, DeLuca as modified teaches the digital
signal processor having at least two output pins where the first pin provides a clock
signal and the second pin provides a disable signal and the state of the disable signal at
the rising edges of the clock signal re read by the converter (Seo, column 2 lines 62-66,
column 3 lines 14-18).

14.   With regards to claims 9 and 14, DeLuca as modified teaches an analog amplifier
operable to receive the disable signal after analog conversion (Seo, Figure 1).

15.   With regards to claim 18, DeLuca as modified teaches the generating of a power-
save signal (Seo, column 3 lines 42-44) where the disable signal is generated in
response to the power-save signal (Seo, column 3 lines 50-54).

16.   With regards to claim 21, DeLuca as modified teaches one of the sleep
conditions is usage of the electronic device (DeLuca, column 7 lines 30-52).

17.   With regards to claim 22, DeLuca as modified teaches the electronic device

being a music player, video player, or multimedia file player (DeLuca, column 5 lines 8-

22).

18.   Claims 19-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over

DeLuca et al US Patent No 5,612,682, Seo et al US Patent No 5,063,597, Tran US

Patent No. 5,734,729, and Nagata US Patent No. 6,114,981 as applied to claim 12

above, and further in view of Lipovski US Patent No 6,675,002.

19.   With regards to claims 19-20, DeLuca as modified fails to teach the generating of

an override signal in response to a disable signal. Lipovski teaches the generating of

an override signal in response to the step of generating a disable signal and terminating

the muting step in response to the override signal (Lipovski, column 6 lines 33-44). At

the time the invention was made, it would have been obvious to a person of ordinary

skill in the art to utilize Lipovski's method of overriding a disable signal because it offers

the advantage of allowing sound output in the event of an emergency (Lipovski, column

6 lines 33-36).

20.   Claim 23 is rejected under 35 U.S.C. 103(a) as being unpatentable over DeLuca

et al US Patent No 5,612,682, Seo et al US Patent No 5,063,597, Tran US Patent No.

5,734,729, and Nagata US Patent No. 6,114,981 as applied to claim 12 above, and

further in view of Fette et al US Patent No. 6,052,600.

21.   With regards to claim 23, DeLuca as modified teaches selecting a data file (Tran,

column 5 lines 8-22), but fails to teach performing a hash function on the data file by the

DSP. However, Fette teaches performing a hashing function on the data to generate

the mathematical function result wherein the hashing function is executed by the digital

signal processor (Fette, column 6 lines 31-45, processor is a DSP, column 9 lines 5-15,

hash of the software program to compare to a predetermined hash). At the time the

invention was made, it would have been obvious to a person of ordinary skill in the art to

utilize Fette's hashing method with DeLuca as modified because it offers the advantage

of providing assurances that files are uncorrupted and that the file will act to

predetermined specifications (Fette, column 2 lines 1-7).

Conclusion

22.   Any inquiry concerning this communication or earlier communications from the

examiner should be directed to Andrew L. Nalven whose telephone number is 571 272

3839. The examiner can normally be reached on Monday - Thursday 8-6, Alternate

Fridays.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, Kambiz Zand can be reached on 571 272 3811. The fax phone number for

the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the

Patent Application Information Retrieval (PAIR) system. Status information for

published applications may be obtained from either Private PAIR or Public PAIR.

Status information for unpublished applications is available through Private PAIR only.

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you have questions on access to the Private PAIR system, contact the Electronic

Business Center (EBC) at 866-217-9197 (toll-free).

Andrew Nalven